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# Detection of Electromigration in Integrated Circuits

AzTE Case #M01-063

## Background

As a result of the high current density running through integrated circuit interconnects, metal atoms in the conductor migrate from their positions and create voids in the material. As these voids form, the voids increasingly degrade the material until the interconnect fails.

### **Invention Description**

Researchers at Arizona State University have developed a new technique to detect the onset of this electromigration and its precise location within the wafer area. The technique employs a pair of conductive traces deposited on the substrate and a multiplicity of conductors connected along the length of the traces. By passing a current between the traces and continuously monitoring the resistances of the traces from one conductor to another, the incidence of resistance changes across any pair of conductors precisely reveals the location of the onset of electromigration.

## **Potential Applications**

- This technology can be used in collaboration with new technologies such as 'self-healing' chips. As feature size decreases, the effect of electromigration increases and consequently, new technologies can improve the reliability of the chips.
- Real-time monitoring of electromigration on ICs can provide a means to study the factors influencing electromigration during its actual life span. Such studies can improve future stages of design.

#### **Benefits and Advantages**

- Helps determine the exact location of the onset of electromigration.
- Real time monitoring of electromigration is possible by integrating the measuring circuitry directly into the semiconductor material.
- The number of segments into which the metal trace is divided does not constitute a limitation. Hence, we can get a high level of accuracy.
- The metallic composition of the interconnects or type of substrate does not constitute a limitation.
- The approach of this invention allows for the model to be consistent across all device topographies such as wafer level, circuit and package parts.

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## Intellectual Property Status:

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