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SiGeSn Buffer Layers for Integration of III-V & II-VI Compound Semiconductors with Silicon

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Patent pending

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Background

Current commercial and defense electronics are based on Silicon (Si) while most RF and optical sources and detectors are based on III-V and II-VI semiconductors grown on non-Si substrates such as GaAs, InP, InAs, GaSb, and CdZnTe. This partitioning of the substrates poses major obstacles to device integration and restricts the choice of material systems that are candidates for bandgap engineering of future devices.

Invention Description

To overcome these problems, this invention utilizes new methodologies for integration of III-V and II-VI compound semiconductors with Si via buffer layers based on novel Si-Ge-Sn alloys. In these methods, the lattice and the thermal expansion coefficient are simultaneously adjusted with composition to match those lattices and coefficients of the desired semiconductor. The buffer layers also provide a mechanism for suppression of threading defects in the overgrowth, resulting in low defect density and smooth surface morphology, which subsequently obviates post-growth chemical mechanical polishing treatments. The technology also provides low growth temperature (<450°C) and short deposition times to allow growth on preprocessed Si wafers.

Potential Applications

- A low-cost, high quality substrate for HgCdTe infrared devices
- Integration of (In,Ga,Al)(P,As,Sb)-based optoelectronics and electronics with Si wafers and Si-based circuitry

Benefits and Advantages

A low-cost and flexible buffer technology for device integration offering:

- Widely tunable lattice constant
- Widely tunable coefficient of thermal expansion (CTE)
- A mechanism for suppressing threading defects in overgrowth
- Very low defect densities and smooth surface morphology
- Compatible with Si CMOS processing for integration of electronic and optoelectronic devices