AzTE Arizona Technology Enterprises

www.azte.com

Reverse Body Bias for Improved Integrated Circuit Total Ionizing Dose Response

AzTE Case # M07-045

Inventors

Dr. Lawrence Clark

Associate Professor
Digital VLSI Laboratory
School of Electrical Engineering
Arizona State University

Dr. Keith Holbert

Associate Professor
Digital VLSI Laboratory
School of Electrical Engineering
Arizona State University

Karl Mohr

Graduate Research Assistant
Digital VLSI Laboratory
School of Electrical Engineering
Arizona State University

Intellectual Property Status:

Patent Pending

Contact

Bill Loux
Director of Business Development
Arizona Technology Enterprises, LLC (AzTE)
480.884.1996 main
480.884.1992 desk
Email: bloux@azte.com

Background

It is possible to fabricate radiation-hardened circuits using commercially available, state-of-the-art CMOS manufacturing processes via novel applications of Radiation Hardening by Design (RHBD) techniques. RHBD techniques allow users to mitigate total ionizing dose (TID) effects caused by layout techniques while being able to handle single event effects (SEE) via a combination of layout and circuit design; however, contemporary RHBD techniques have their limits. For example, while dual interlocked storage cells (DICE) latches can mitigate the effects of single event upsets (SEU), these latches can be vulnerable to single event transients (SET). Temporal latches, on the other hand, are capable of mitigating both SEU and SET effects but only at the cost of increased circuit area, circuit setup time, and power consumption. Meanwhile, using annular logic gates can worsen Energy Delay Product (EDP) somewhere between 35%-350%.

Invention Description

Researchers at Arizona State University have developed a new design technique for RHBD designs that addresses shortcomings of current RHBD techniques. Reverse Body Bias is a technique that introduces an alternative path for leakage to follow rather than leaving it to disrupt any logic. The new design technique utilizes proven hardening techniques while offering lower power consumption and smaller circuits. The novel design technique focuses on mitigating the effects of SEEs while also maintaining hardness against radiation effects in general.

Potential Applications

- **Satellites**
- **Space Exploration**
- **Nuclear Environments**
- **Defense**

Benefits and Advantages

- **Circuit Area –** over 25% reduction compared to traditional methods
- **Energy Delay Product –** comparable to traditional methods and 35%-350% better than “annular” methods
- **Leakage –** allows less chip-level leakage
- **Manufacturability –** relies on available standard CMOS fabrication processes