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Methods and Compositions for Preparing Tensile Strained Ge on $Ge_{1-y}Sn_y$ Buffered Semiconductor Substrates

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Inventors

John Kouvetakis

Professor

Department of Chemistry and Biochemistry

Yan-Yan Fang

Graduate Student

Department of Physics

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Contact

Bill Loux

Director of Business Development

Arizona Technology Enterprises, LLC (AzTE)

480.884.1996 main

480.884.1992 desk

Email: bloux@azte.com

Background

Germanium (Ge) has a direct band gap (E_0) of 0.81 eV at room temperature; however, applying small perturbations to Ge can shift E_0 to lower energies resulting in dramatically improved performance for semiconductor and telecommunication applications. Stressing Ge using tensile strain provides one means by which to lower its E_0, but the current best method requires depositing the Ge on Silicon (Si) at relatively high temperatures and inducing stress through the subsequent contraction of the Si. While this process provides biaxial tensile strains as high as 0.25% in films as thick as 1 µm, higher strain values are necessary for most optoelectronic applications, which require tunable E_0. Furthermore, the thermal expansion process lacks precise strain control, offers limited maximum strain value (~0.3%), and effectuates undesirable inter-diffusion of the elements across the Si-Ge heterojunction.

Invention Description

Researchers at Arizona State University have developed an improved method for preparing tensile strained Ge on semiconductor substrates. Specifically, this method forms a tensile strained layer of Ge over a layer of $Ge_{1-y}Sn_y$ deposited on a semiconductor substrate using an admixture of $(GeH_3)_2CH_2$ and Ge_2H_6 in a ratio of between 1:10 and 1:30. The tensile strained. The method functions to tune the strain of the Ge epilayer by varying the buffer composition.

Potential Applications

- **Semiconductor Electronics** (e.g. high-speed transistors, back-end CMOS telecommunications, etc.)
- **Optoelectronics** (e.g. Optical Fiber Communications, Lasers, etc.)

Benefits and Advantages

- **Tunable Tensile Strains** (between 0.15% and 0.45%) – precise strain control for optoelectronic applications
- **Increased Maximum Tensile Strain** (high as 0.45% observed compared to 0.3%) – necessary for viability in higher bands (e.g. U-Band)
- **Operates at Substantially Lower Temperatures** (growth occurs at 350-380°C as opposed to 800-900°C) **–** reduces inter-diffusion of the elements across the Si-Ge heterojunction; CMOS compatible
- **Offers High-Quality, Thermally Stable Tensile Strained Ge Layers** (greater than 100 nm thick have been grown on Si(100) wafers)
- **Exhibits Desirable Crystalline Geometry** – perfectly tetragonal structure, homogenous compositional and strain profiles, low threading dislocation densities and atomically planar surfaces; optimal for tuning applications