



Analog Return Loss Detection and Matching State Searching Circuit for Automatic Antenna Impedance Tuning System

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Background

Before converting detected power levels to the digital domain, conventional antenna tuning systems couple incident and reflected powers through a three-line directional coupler in addition to two RF power detectors. Replacing these conventional antenna tuning systems with the automatic antenna matching techniques and devices employed at lower radio frequencies can greatly improve commercial wireless and military communications.

Invention Description

Researchers at ASU have invented a system that effectively utilizes these automatic antenna matching techniques and devices and have reduced the system to practice using discrete components on several printed circuit boards. Specifically, this system employs an analog subtractor by finding the difference between the outputs of two logarithmic power detectors to compute return loss. While the antenna tuning system searches for the optimum matching state, it stores the initial value of return loss and the impedance synthesizer state in an analog sample and hold (S/H) and digital register, respectively. Comparing each new return loss value to the old, the system stores whichever value is larger as well as the associated matching state until finding the optimum matching state. As a result, this system requires no analog to digital convertors (ADC) and consequently, eliminates the cost of high accuracy ADCs, which require moderate power and occupy significant silicon space.

Potential Applications

An analog return loss detection system offers great benefit to the emerging market of software defined radio (SDR), which is expected to grow rapidly in the future.

- **Software Defined Radio architectures**
- **Current automatic antenna tuning schemes**

Benefits and Advantages

- **Accuracy** – By eliminating the ADCs, the quantization accuracy of the ADCs does not limit the accuracy of the circuit.
- **Reduced Clock Cycle** – Impedance state changes each clock cycle to eliminate the tradeoff amongst conversion speed (clock cycles), number of bits (resolution) and power consumption that occurs in ADCs.
- **Simplification** – The simplification of the circuits considerably reduces the power consumption at the same clock frequency as compared to circuits using ADCs.
- **Reduced Silicon Footprint** – Invention simplifies the corresponding integrated circuit design and reduces the silicon area significantly.
- **Return Loss Calculation** – Logarithmic power detectors greatly reduce the requirements for the dynamic range of the following stages and simplify the calculation of return loss significantly.