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Lightweight Error Detection and Correction for Semiconductor Memories

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Intellectual Property Status

Patent Pending

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Background

Microprocessors depend on high integrity instructions and data to function properly. Various factors can corrupt this information, with high-energy sub-atomic particles and other types of electromagnetic radiation effects being among the more difficult of these factors against which to guard. Because a single erroneous bit of information can lead to significant operation errors, processors may employ error detection and correction (EDAC) techniques to verify the integrity of information prior to use. Indeed, EDAC schemes can even provide an effective safety-guard against radiation effects (radiation hardening).

Still, existing EDAC schemes, while effective, produce performance penalties (e.g. processing, area) that limit the use of EDAC schemes to larger memories and second layer (L2) cache of high performance processor applications. These performance penalties generally preclude the use of EDAC schemes in register files and limit the application of EDAC schemes in first level (L1) caches. Consequently, many processors must rely on error detection schemes alone, reserving employment of EDAC schemes for memories where processor overhead, access speeds, and overall size have limited importance.

Accordingly, there is a need for an EDAC scheme that is significantly more efficient than conventional EDAC schemes. Moreover, for environments subject to radiation, there is also a need for an efficient and effective EDAC scheme that is conducive to radiation hardening.

Invention Description

Researchers at Arizona State University have developed a novel lightweight EDAC scheme that employs a two-dimensional parity technique to reduce area and timing overhead penalties. The technique is appropriate for high speed memory structures such as register files and L1 caches and provides radiation hardening by design.

Potential Applications

- **Integrated Circuits** (e.g. Microprocessors, etc.)
  - **High Speed Memory Structures** (e.g. Register Files, Caches, etc.)
- **Radiation Hardening** (e.g. Satellites, Space Exploration, Defense, etc.)

Benefits and Advantages

- **Provides Lightweight Error Detection and Correction** –
  - Reduces area and timing overhead penalties of conventional EDAC schemes through the simplicity of the parity scheme; area overhead varies between 2% and 12.7%, compared with 4% to 62.5%, depending on code word row width
  - Suitable for small, fast arrays such as register files and L1 caches that require low read and write latency as well as small write granularity
- **Provides Radiation Hardening by Design**
  - Mitigated 100% of soft-errors using appropriate bit interleaving during accelerated heavy ion testing
  - Allows fabrication of hardened circuits from commercially available state-of- the-art CMOS manufacturing processes
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