A Robust Edge-Triggered Threshold Logic Flipflop (PNAND) with Scan, Preset, and Clear Functions
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Background
Digital circuits use sequences of logic gates called flip-flops to store and transmit binary information. A NAND is a multi-input flip-flop that produces a false output only if all its inputs are true, and can therefore be used to process any other logic function. A threshold logic flip-flop can compute a single input function like an ordinary D-type flip-flop, as well as complex multi-input functions that would otherwise require multiple D-type flip-flops. As a result, digital circuits made from threshold logic flip-flops are smaller, faster, and more power efficient. However, current threshold logic flip-flops suffer a disproportionally large clock load for a higher number of inputs, allow variable loading that can cause clock timing issues, and have no failsafe to prevent the occurrence of a floating node.

Invention Description
Researchers at ASU have developed PNAND, a multi-input flip-flop circuit that computes a threshold logic function using differential signaling. Differential signaling resists electromagnetic interference by detecting the difference between two complementary signals. PNAND eliminates the possibility of a floating node by applying positive feedback between two input signals to ensure neither node falls into an indeterminate state. PNAND’s input capacitance is substantially lower and is independent of the input, reducing clock demand and restricting timing variability. Instead of only producing outputs synchronous to clock, PNAND behaves like a scan clock whenever test enable is asserted or dropped. This is considerably less intrusive in terms of power and delay and produces clearer results when tested for quality. Additionally, an asynchronous preset-and-clear mechanism simultaneously sets or resets all of PNAND’s latches and on top of that has reduced power use and delay time in operation.

Potential Applications
- Digital Circuits
- DSP Cores
- Microelectronics
- Microprocessors

Benefits and Advantages
- **Accurate**
  - Failsafe for floating node ensures that there is no soft error (incorrect signal).
  - Less intrusive scan functionality allows for superior quality control.
- **Efficient** – Low and independent input capacitance reduces power consumption without penalizing performance, resulting in smaller, faster circuits.
- **Practical**
  - Implements simple, single-input and complex multi-input logic functions.
  - Asynchronous preset-and-clear simultaneously sets or resets all latches.
- **Reliable** – Withstands electromagnetic interference by differential signaling.