AzTE
ASU® TECHNOLOGY TRANSFER

Optimized Multi-Channel BCH Decoder

AzTE Case #M15-265P

Inventors

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Background

Error rates in storage and communication channels are increasing as technology advances. Computer programmers design certain types of code called BCH code to detect and correct these errors. In comparison with writing the code, decoding is more complex due to a decoder's throughput (performance), operation, and area. Clock speed (the decoder's registry quickness) and bit-parallel operation (concurrently working with multiple bits) limit the decoder's throughput. Implementing bit-parallel operation increases the needed area and limits the number of errors the decoder can correct, making it difficult to achieve higher clock speeds. Therefore, researchers now look to develop a hardware-efficient BCH decoder with more space for bit-parallel operation to improve overall throughput.

Invention Description

ASU researchers have developed a multi-channel BCH error-correction decoder that improves hardware productivity, creating significant savings in area and power while allowing a negligible performance reduction. As the decoder sifts through data, it produces a set of vectors as a function of error locations (the syndrome calculation). Thereafter, it generates and factors a polynomial to the roots that give the error locations. In order to make more area, researchers eliminated the decoder's excess calculations. Through using a pooled group approach (funneling data to the first available decoding unit), the decoder reduces hardware area by 47%-71% and increases dynamic power by 44%-59%. Overall, the BCH decoder optimizes hardware usage and promotes huge savings in area and power with an insignificant reduction in performance.

Intellectual Property Status:

Pending

Potential Applications

- Decoding Software
- Storage Controllers (SSD, MMC, NAND, etc.)
- Communications Controllers (satellite, radio, cellular, etc.)
- Microcontrollers

Benefits and Advantages

- **Efficient** – optimized hardware usage generates savings in area around 47%-71% with possible increases in dynamic power around 44%-59%
- **Lower Cost** – the decoder's simplified calculations extend to bit-parallel support, mitigating the need for expensive root-finding methods
- **Customizable** – area-efficiency makes space to condense additional decoders onto the same area for diverse industry needs

Contact

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