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Sample-time Calibration of Time Interleaved Analog-to-Digital Data Converters

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Inventors

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Background

Time-interleaving increases the effective data conversion rate in analog-to-digital converters (ADC) without sacrificing speed. To conserve power, time interleaving is used with multiple parallel paths to process a signal at a frequency using a multiplexed approach at a lower frequency. However, this technique faces design challenges due to the parallel identical channels and complex circuitry. The most significant issue is the timing mismatch between channels, also called sample-time error. This can directly affect the performance of the ADC by creating a mismatch between channels in the sample-time. This sample-time error generates an unwanted spur in the frequency spectrum of the overall signal. Current techniques to solve this problem use complicated detection methods, such as the Hilber transform. However, the complexities of these methods limit their application. Therefore, there is a need for a simplified technique to resolve sample-time errors in time-interleaved analog-to-digital converters.

Invention Description

Researchers at Arizona State University have introduced a novel mixed-signal scheme for the sample-time error calibration in time-interleaved analog-to-digital converters (TIADC). Interchannel equalization is used to remove the sample-time error mismatch between channels by using an extra channel. This technique is used to suppress the unwanted image due to the sample-time error between channels. This can effectively decrease the complexity of the calibration engine compared to previous techniques, thus saving power and area in the overall ADC. This process can be repeated during signal processing so as to recalibrate to account for any performance drift. This allows sample-time mismatch to be removed.

Intellectual Property Status:

Pending

Potential Applications

- Analog-to-Digital Converters
- Time interleaving systems

Benefits and Advantages

- **Simplified Technique** – Reduces the complexity of the system by using an extra channel.
- **Improved SNDR** - Simulation results show that this technique is able to improve the signal-to-noise-plus-distortion ratio (SNDR) for a 12-bit TIADC system by 29 dB at 37% of the Nyquist rate frequency.
- **Conserves Energy** – The simplicity of the system saves power without compromising speed or performance.

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